

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claim 4 without prejudice and amend claim 3 as follows:

LISTING OF CLAIMS:

1-2. (Canceled)

3. (Currently Amended) A trace control circuit comprising:

address capturing means for capturing a relative address in a
memory accessed by a CPU;
data capturing means for capturing access data of the CPU; [[and]]
output means for outputting a reference address to a trace bus and
outputting the relative address in the memory captured by the address capturing
means and the access data captured by the data capturing means; and
determining means for determining whether the CPU outputs the
relative address in the memory or the absolute address thereof, and for requesting
the address capturing means to capture one of the relative address and the absolute
address.

4. (Canceled)

5. (Original) A trace control circuit comprising:

address capturing means for capturing an address in a memory
accessed by a CPU;

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data capturing means for capturing data for block transfer; and
output means for outputting to a trace bus the address captured by
the address capturing means and the data captured by the data capturing means
upon a first access in the block transfer, and for outputting the data captured by the
data capturing means to the trace bus upon a second and subsequent accesses.

6. (Original) The trace control circuit according to claim 5, wherein the
output means outputs a reference address to the trace bus, when the address
captured by the address capturing means is a relative address.